IN THE CLAIMS

Please cancel without prejudice claims 1-20.

Please add new claims 21-40 as indicated below.

1. – 20. (Cancelled).

21. (New) A method, comprising:

receiving, at a memory module controller of a memory module having a plurality of memory devices, a memory request signal from a system memory controller over a system memory bus; and

in response to the memory request signal, having the memory module controller, which serves as an interface between the plurality of the memory devices and the system memory bus, to generate a separate signal addressed to and serviced by at least one of the plurality of memory devices in a manner specifically required by a specification of the plurality of memory devices, such that the plurality of memory devices and the system memory bus operate in different operating environments.

22. (New) The method of claim 21, further comprising generating a separate clock signal via a clock generator within the memory module controller to drive the separate signal, the separate clock signal being different than a clock signal of the system memory bus.

23. (New) The method of claim 21, further comprising:

examining the memory request signal to determine whether the memory request signal is addressed to at least one of the memory devices of the respective memory module; and

bypassing the memory request signal if the memory request signal is not addressed to any of the memory devices of the memory module.

24. (New) The method of claim 23, further comprising reducing at least a portion of a power associated with the plurality of memory devices if the memory request signal is not addressed to any of the memory devices.

25. (New) The method of claim 23, further comprising reducing a frequency of the separate clock signal with respect to the plurality of memory devices if the memory request signal is not addressed to any of the memory devices.

C1 cont'd

26. (New) The method of claim 23, further comprising decoupling the plurality of memory devices from the system memory bus if the memory request signal is not addressed to any of the memory devices, such that the plurality of memory devices remain inactive.

27. (New) The method of claim 23, further comprising providing the separate clock signal and power to the memory devices of the memory module only if the memory request signal is addressed to at least one of the memory devices.

28. (New) The method of claim 21, wherein the plurality of memory devices and the system memory controller operate at different power voltages.

29. (New) The method of claim 21, wherein the plurality of memory devices and the memory controller operate at different operating frequency signals having different voltage swings.

30. (New) A system, comprising:

a memory bus;

a system memory controller coupled to the memory bus; and

a first memory module coupled to the memory bus, the first memory module including

a first plurality of memory devices and

a first memory module controller coupled to the first plurality of memory devices and the memory bus to receive a memory request signal from the system memory controller via the memory bus,

in response to the memory request signal, the first memory module controller, which serves as an interface between the first plurality of memory devices and the memory bus, to generate a separate signal addressed to and serviced by at least one of the plurality of memory devices in a manner specifically required by a specification of the plurality of memory devices, such that the first plurality of memory devices and the system memory controller operate in different operating environments.

C 1 Cont'd

31. (New) The system of claim 30, wherein the first memory module controller further comprises a clock generator to generate a clock signal to drive the separate signal, wherein the clock signal is different than a clock signal of the memory bus.

32. (New) The system of claim 31, wherein first memory module controller further comprises a request handling logic to examine the memory request to determine whether the memory request is addressed to at least one of the memory devices and to ignore the memory request if the memory request is not addressed to any of the memory devices.

33. (New) The system of claim 32, wherein the first memory module controller further comprises a power management unit to control a power supplied to the memory devices.

34. (New) The system of claim 33, wherein the first plurality of memory devices and the memory bus operate at different power voltages.

35. (New) The system of claim 33, wherein the power management unit reduces at least a portion of the power to the memory devices, if the memory request is not addressed to any of the memory devices.

C1 cont'd

36. (New) The system of claim 33, wherein the first memory module controller further comprises a control logic coupled to the request handling logic, the clock generator, and the power management unit, the control logic configured to decouple the memory devices from the memory bus if the memory request is not addressed to any of the memory devices.

37. (New) The system of claim 36, wherein in response to a signal from the request handling logic indicating that the memory request is not addressed to any of the memory devices, the control logic instructs the clock generator to alter a frequency of the clock signal to the memory devices.

38. (New) The system of claim 37, wherein the control logic further instructs the power management unit to disable the clock generator if the memory request is not addressed to any of the memory devices, which in turn reduces the power dissipation of the memory devices.

39. (New) The system of claim 30, further comprising a second memory module coupled to the memory bus, the second memory module including:

a second plurality of memory devices and

a second memory module controller coupled to the second plurality of memory devices and the memory bus, the second memory module controller managing the second plurality of memory devices in dependent of the first memory module controller of the first memory module.

C1 cont'd

40. (New) The system of claim 39, wherein the first plurality of memory devices and the second plurality of memory devices have different characteristics, which are controlled by the first and second memory module controllers respectively.